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| 10/696,146 | 10/29/2003 | Michael B. Galles | 062986.0296 | 5506 |

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| EXAMINER | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

| Notification of Non-Compliant Appeal Brief (37 CFR 41.37) | Application No. 10/696,146 | Applicant(s) GALLES ET AL. | |
|---|---|---|---|
| | Examiner William M. Treat | Art Unit 2181 | |

*--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

The Appeal Brief filed on *29 August 2007* is defective for failure to comply with one or more provisions of 37 CFR 41.37.

To avoid dismissal of the appeal, applicant must file anamended brief or other appropriate correction (see MPEP 1205.03) within **ONE MONTH or THIRTY DAYS** from the mailing date of this Notification, whichever is longer. **EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136.**

1. ☐ The brief does not contain the items required under 37 CFR 41.37(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, (e.g., rejected, allowed, withdrawn, objected to, canceled), or does not identify the appealed claims (37 CFR 41.37(c)(1)(iii)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 41.37(c)(1)(iv)).

4. ☐ (a) The brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings, if any, by reference characters; and/or (b) the brief fails to: (1) identify, for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function under 35 U.S.C. 112, sixth paragraph, and/or (2) set forth the structure, material, or acts described in the specification as corresponding to each claimed function with reference to the specification by page and line number, and to the drawings, if any, by reference characters (37 CFR 41.37(c)(1)(v)).

5. ☐ The brief does not contain a concise statement of each ground of rejection presented for review (37 CFR 41.37(c)(1)(vi))

6. ☐ The brief does not present an argument under a separate heading for each ground of rejection on appeal (37 CFR 41.37(c)(1)(vii)).

7. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 41.37(c)(1)(viii)).

8. ☐ The brief does not contain copies of the evidence submitted under 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner **and relied upon by appellant in the appeal**, along with a statement setting forth where in the record that evidence was entered by the examiner, as an appendix thereto (37 CFR 41.37(c)(1)(ix)).

9. ☐ The brief does not contain copies of the decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief as an appendix thereto (37 CFR 41.37(c)(1)(x)).

10. ☒ Other (including any explanation in support of the above items):

*See attached.*

NOTIFICATION OF NON-COMPLIANCE WITH THE REQUIREMENTS OF 37 CFR 41.37(c)

1. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

2. On 6/23/2005 applicants amended their independent claim 1 in 10/696,146, in conjunction with filing an RCE, to recite: "A multi-processor system, comprising: a plurality of processors, each processor including an integrated memory operable to provide/receive/store data, each processor **including a central processing unit** having an integrated memory controller operable to control access to the integrated memory, ~~each processor including~~ **and** an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory; ..." Applicants amended independent claim 16 to recite: "A processor in a multi-processor system, comprising: a local memory integrated in the processor and operable to provide/receive/store data; **a central processing unit;** a memory controller integrated in the ~~processor~~ **central processing unit** and operable to control access to and from the local memory; a memory directory integrated in the ~~processor~~ **central processing unit** and operable to maintain memory references to data within the local memory ... " Following making this amendment applicants argued in relation to the 102 rejection over the Kabemoto patent: "Independent Claim 1 recites 'each processor including an integrated memory operable to provide/receive/store data, each processor including a

central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory ' By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, a directory memory is disclosed as being separate and apart from the processor." Applicants also argued in relation to the 102 rejection over the Chase patent: "Independent Claim 1 recites ' ... each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory.' By contrast, the station 12 of the Chase, et al. patent equated by the Examiner as the claimed processor shows a processor 18 and a storage 21 with a cache 20 separate and apart from its processor 18. Thus, the storage 21 and cache 20 of the Chase, et al. patent are not integrated within its processor 18 as would be required by the claimed invention." In support of such arguments applicants have referred the examiner to applicants' specification where it states in relation to Fig. 1: "Each of the plurality of processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all integrated into a single device."

3. Applicants have never offered a clear definition in their disclosure or their arguments for the term, "integrated" though the implied definition based on their arguments seems to be that the elements which are integrated must be on the same

computer chip or integrated circuit (IC). By the end of 1998 there were more than 100,000 patents in the U.S. Patents data base which used the terms, computer chip(s) or integrated circuit(s). If applicants meant that the elements which are integrated must be on the same computer chip or integrated circuit, as individuals of ordinary skill in the art, they certainly knew how to say so as did thousands of other inventors. Instead of saying "Each of the plurality of processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all integrated into a **single integrated circuit device or single integrated circuit or single computer chip**", applicants chose to say "Each of the plurality of processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all **integrated into a single device**."

4. Applicants and the examiner have argued throughout the prosecution of the current application about the meaning of the word "integrated" as in "Each of the plurality of processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all integrated into a single device." The examiner's copy of Webster's Ninth New Collegiate Dictionary, published in 1990, offers the following definition for **integrate**: "to form, coordinate, or blend into a functioning whole". The examiner's copy of Webster's Ninth New Collegiate Dictionary also offers the following definition for **device**: "a piece of equipment or a mechanism designed to serve a special purpose or a mechanism designed to serve a special purpose or perform a special function." The examiner's second edition of the Microsoft Press Computer Dictionary, published in 1994, offers the following definition for **integration**: "In computing, the combining of different activities, programs, or hardware components into a functional

unit." As the examiner has pointed out throughout the prosecution there is no definition of integrated anywhere in applicants' disclosure which would prevent the examiner from giving the term, integrated, its broadest reasonable interpretation, and the same applies to the word, device.

5. In response to applicants' argument that "Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor", the examiner has consistently pointed out applicants' original disclosure never offered a definition for integrated. And, while Fig. 1 shows a dotted line around relevant components labeled "'processor" there is nothing in applicants' original disclosure to limit such components to the same computer chip or the same computer board, or same external housing, or same rack, or same room, etc. Applicants' Fig. 1 provides no definition for the term integrated other than to say the components depicted work with one another in terms of hardware and software as a single device as do Chase's relevant components and Kabemoto's relevant components

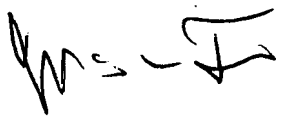
6. Applicants have never offered a specific definition for "integrated" nor have they explained why the examiner's interpretation of the meaning of the claim language is unreasonable and inappropriate. If the examiner's interpretation of applicants' claim language is reasonable and appropriate, applicants arguments for the patentability of their claims fail to explain how applicants' claim language avoids the references and the examiner's arguments. Please make clear why the examiner's interpretation of applicants' claim language is unreasonable and inappropriate or provide new arguments

which make clear how applicants' claim language avoids the references and the examiner's arguments.

7. In that applicants are insisting on amending their original disclosure in a manner inconsistent with the scope of applicants' parent application (09/418,520), which has become Patent No. 6,651,157, applicants might also consider explaining why they think the examiner should not require applicants to file a new oath or declaration and indicate that the application is a continuation-in-part (MPEP 602.05(a), last two sentences of the first paragraph). Note that in the 8 years since Patent No. 6,651,157 was originally filed as Application No. 09/418,520, applicants have never sought to make similar amendments to the parent application or patent which would maintain consistency of scope between the two applications.

8. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER